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06ES32

Third Semester B.E. Degree Examination, June 2012

Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is transition and diffusion capacitance? State the expressions for both and explain the terms. **(06 Marks)**

b. For the diode clipping circuit shown in Fig. Q1 (b), sketch the input and output waveforms for R = 10 K for $v_i = 20\sin\omega t$ and $v_R = 10V$. Assume $R_f = 100\Omega$, $R_r = \infty$ and $V_r = 0$. **(06 Marks)**

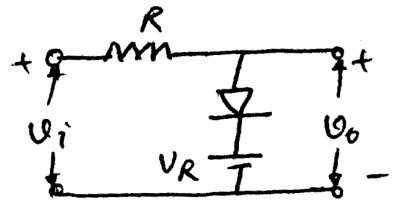

Fig. Q1 (b)

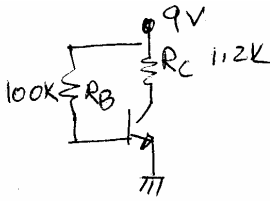

Fig. Q2 (b)

c. What is a clamper circuit? With circuit diagram explain the working of simple negative Clamper. Also sketch the output waveform for the sinusoidal input. Also sketch positive clamper. **(08 Marks)**

2 a. Explain the factors against which an amplifier needs to be stabilized. Define the stability factor $S(I_{CO})$. Calculate ΔI_C, if $\Delta I_{CO} = 100\mu A$, $S(I_{CO}) = 5$. **(06 Marks)**

b. For the circuit shown in Fig. Q2 (b), calculate I_B, I_C, I_E and V_{CE}. Assume $\beta = 45^\circ$ and $V_{BE} = 0.7$ **(06 Marks)**

c. Name different biasing methods of transistor. With the circuit diagram analyze how stability is achieved by collector to base bias circuit. **(08 Marks)**

3 a. Given $I_E = 3.2$ mA, $h_{fe} = 150$, $h_{oe} = 25$ μmho and $h_{ob} = 0.5$ μmho. Determine and draw

i) The common-emitter hybrid equivalent circuit.

ii) The common-base r_e model. **(07 Marks)**

b. For the network shown in Fig. Q3 (b),

i) Determine r_e.

ii) Find Z_i (with $r_0 = \infty\Omega$)

iii) Calculate z_0 (with $r_0 = \infty\Omega$)

iv) Determine Av (with $r_0 = \infty\Omega$). Assume β = 100. **(08 Marks)**

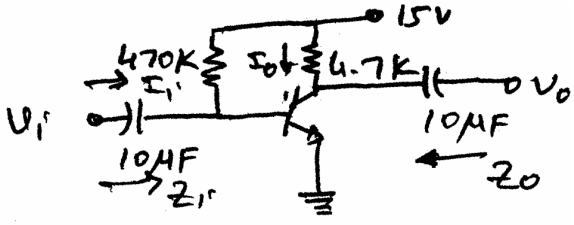

Fig. Q3 (b)

c. Compare common emitter, common-base and common collector configured transistor amplifier with respect to impedance, voltage gain, current gain and phase shift. **(05 Marks)**

4 a. Draw the single stage-RC coupled BJT amplifier and discuss the effect of,
i) Input capacitor C_s,
ii) Emitter bypass capacitor C_e and
iii) Output capacitor, C_c on frequency response. **(10 Marks)**

b. Four identical non-interacting cascades stages have an overall upper 3 dB frequency of 50 kHz and a lower 3 dB frequency of 50 Hz. Determine f_L and f_H of each stage. Also find the bandwidth of each stage. **(05 Marks)**

c. Prove that Miller effect capacitance, $C_{Mi} = (1 - A_V)Cf$ **(05 Marks)**

PART – B

5 a. With the help of circuit diagram discuss the importance of,
i) Cascode connection and
ii) Darlington connection. **(08 Marks)**

b. Name four basic ways of connecting the feedback signal. Draw their block diagrams, indicating input and out signals, the forward and feedback path gain. **(08 Marks)**

c. Derive an expression for input impedance of an voltage-series feedback amplifier. **(04 Marks)**

6 a. For a power amplifier circuit shown in Fig. Q6 (a), supplied with input voltage that results in a base current of 10 mA peak. Determine the i) input power ii) output power and iii) efficiency. **(08 Marks)**

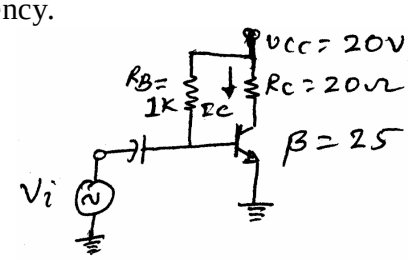

Fig. Q6 (a)

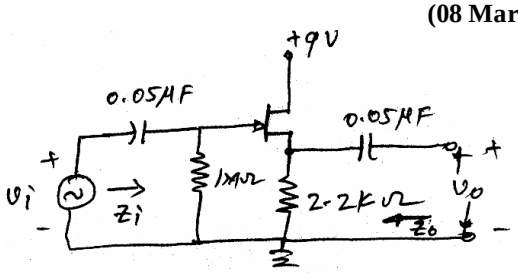

Fig. Q8 (b)

b. Draw the transformer-coupled class A amplifier circuit and discuss
i) Transformer action ii) Voltage transformation iii) Current transformation and iv) Impedance transformation in terms of turns ratio. **(08 Marks)**

c. Write a note on amplifier distortion and harmonics in power amplifier circuits. **(04 Marks)**

7 a. With the help of block diagram, explain the oscillator operation. **(06 Marks)**

b. With the help of circuit diagram, explain the working of Colpits oscillator. For the circuit $C_1=C_2=C$ and L = 100μH, frequency of oscillation is 500 kHz. Determine value of C_{eQ}. **(10 Marks)**

c. A crystal has L = 0.4 H, C = 0.085 PF and CM = 1 PF with R = 5 KΩ, find
i) Series resonant frequency
ii) Parallel resonant frequency and
iii) Quality factor of crystal. **(04 Marks)**

8 a. With the help of circuit diagram of JFET self-bias configuration and its equivalent circuit derive an expression for,
i) input impedance, z_i
ii) output impedance and
iii) voltage gain, Av
(Assume Rs is bypassed with Cs). **(10 Marks)**

b. The network shown in Fig. Q8 (b) has $V_{GSQ} = -2.86V$, I_{DQ} = 4.56mA, I_{DSS} = 16 mA, V_P = -4 V and Y_{OS} = 30 μS. Determine i) g_m ii) r_d iii) Z_i iv) Z_o without r_d and v) A_v without rd. **(10 Marks)**

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